```
File 347:JAPIO Nov 1976-[redacted]4/Feb(Updated 040607)
         (c) 2004 JPO & JAPIO
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200437
         (c) 2004  Thomson Derwent

Set     Items   Description
S1        151   (ENDIAN? OR ORDER???(3N)BYTE? ?)(10N)(CONVERT? OR CONVERSI-
                ON OR TRANSFORM? OR TRANSLAT? OR CHANG??? OR EXCHANG??? OR SW-
                ITCH??? OR SWAP???? OR MODIF???? OR MODIFICATION? ? OR ALTER?-
                ?? OR ALTERATION? ? OR FLIP????)
S2         41   SWAP????(5N)BYTE? ?
S3      41982   HEADER? ?
S4       8370   LUT OR LUTS OR (LOOKUP OR LOOK()UP)()TABLE? ?
S5          ?   S1:S2 AND S3
S6          )   S1:S2 AND S4
S7         13   S1:S2 AND TABLE? ?
S8     207562   FILE? ?(5N)ACCESS??? OR FILESYSTEM? ? OR FILE()SYSTEM? ? OR
                FAT?? OR NTFS
S9          0   S1:S2 AND S8
S10         6   S1:S2 AND FILE? ?
S11        19   S5 OR S7 OR S10
S12       124   ENDIAN?
S13         0   S8 AND S12
S14         0   S4 AND S12
S15         6   S3 AND S12
S16         3   S15 NOT S11
S17        13   (ARRANG?(3N)BYTE? ?)(10N)(CONVERT? OR CONVERSION OR TRANSF-
                ORM? OR TRANSLAT? OR CHANG??? OR EXCHANG??? OR SWITCH??? OR S-
                WAP???? OR MODIF???? OR MODIFICATION? ? OR ALTER??? OR ALTERA-
                TION? ? OR FLIP????)
S18       288   BYTE? ?(5N)(REORDER? OR RE()ORDER??? OR SWITCH??? OR INTER-
                CHANG???)
S19        10   S17:S18 AND S3:S4
S20        13   S17:S18 AND TABLE? ?
S21         0   S17:S18 AND S8
S22        23   S19:S20
S23        18   S22 NOT (S11 OR S16)
```

11/5/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2004 JPO & JAPIO. All rts. reserv.

07756257 **Image available**
DATA PROCESSING METHOD AND DATA PROCESSOR

PUB. NO.: 2003-250163 [JP 2003250163 A]
PUBLISHED: September 05, 2003 (20030905)
INVENTOR(s): SASANO TAKAAKI
MATSUMURA KENZO
ITO HIDEJI
EMATA KOJI
INOUE MANABU
ASANO SHOJI
APPLICANT(s): HITACHI ULSI SYSTEMS CO LTD
APPL. NO.: 2002-049398 [JP 200249398]
FILED: February 26, 2002 (20020226)
INTL CLASS: H04N-009/67; G06F-007/38; G06T-001/00; H04N-001/46; H04N-001/60

ABSTRACT

PROBLEM TO BE SOLVED: To provide a data processing method for performing correction processing of a result of arithmetic operation so as to fall into a prescribed range of numeral values at high speed when the results of arithmetic operations are deviated from the range of numeral values.

SOLUTION: The data processor includes a conversion **table** wherein an optional value can be registered to an address 0, a maximum value 'FFh' of a numeral value range (00h to FFh) is registered from an address 1 to an address X, and a minimum value '00h' of the numeral value range is registered from the address X to the final address, respectively, after a value in 1-byte defined in the numeral value range is obtained by 2-byte arithmetic operations, the low-order 1-byte of the result of arithmetic operations is registered to the address a prescribed of the **conversion table** (step S2), and using the high- **order** 1- **byte** of the result of arithmetic operations for an address to index the registered value from the conversion **table** (step S3) to use the value for a correction value.

COPYRIGHT: (C)2003,JPO

11/5/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2004 JPO & JAPIO. All rts. reserv.

07564520 **Image available**
DATA TRANSFER METHOD AND DATA CONVERTER

PUB. NO.: 2003-058361 [JP 2003058361 A]
PUBLISHED: February 28, 2003 (20030228)
INVENTOR(s): KIM HOMUN
HASHIZUME TATSUNARI
APPLICANT(s): OKI ELECTRIC IND CO LTD
APPL. NO.: 2001-249041 [JP 2001249041]
FILED: August 20, 2001 (20010820)
INTL CLASS: G06F-005/00

ABSTRACT

PROBLEM TO BE SOLVED: To perform data conversion by selecting only a piece of data to which the data **conversion** is required irrespective of difference between the **endians** of master/slave information equipment that perform data communication.

SOLUTION: A CPU 28 of a master 10 refers to a data **table** 30 in which endian information of a slave 12 as a data transfer destination is preliminarily stored and raises a flag only when the data conversion is not required. In a data converter that has received data 24, a decision device

34 sorts the data accord[redacted] to presence/absence of the fl[redacted]nd records the sorted data in an address space 40 or 42. Software 46 read by a CPU 50 of the data converter performs the data conversion to only the data recorded in the address space 40, defines it as converted data 26 and transfers it to the slave 12.

COPYRIGHT: (C)2003,JPO

11/5/3 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2004 JPO & JAPIO. All rts. reserv.

06201405 **Image available**
DATA CONTROLLER

PUB. NO.: 11-149363 [JP 11149363 A]
PUBLISHED: June 02, 1999 (19990602)
INVENTOR(s): KATO HIROYUKI
APPLICANT(s): TOSHIBA CORP
APPL. NO.: 09-318161 [JP 97318161]
FILED: November 19, 1997 (19971119)
INTL CLASS: G06F-005/00

ABSTRACT

PROBLEM TO BE SOLVED: To recognize **endian** setting and to automatically execute **conversion** .

SOLUTION: A ROM controller 107 of a memory controller 104 fetches data from a ROM 108 and discriminates the number of bits in the ROM 108 from fetched data and ROM bit width information in the ROM controller 107 and repeats the fetching of data from the ROM 108 until the bits becomes 32 bits. Obtained data is converted to have proper byte arrangement by which a command can precisely be understood by referring to the command peculiar to a CPU 101, which is preserved in a command **table** 106. When a conversion method is determined, code data from ROM 108 is sequentially converted by a **byte swapping** circuit 105 by the determined method and it is sent to the CPU 101.

COPYRIGHT: (C)1999,JPO

11/5/4 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2004 JPO & JAPIO. All rts. reserv.

05538184 **Image available**
GENERALIZED DATA FORMAT CONVERTING DEVICE

PUB. NO.: 09-152984 [JP 9152984 A]
PUBLISHED: June 10, 1997 (19970610)
INVENTOR(s): TAN PEKU YUU
KEE NUN FUATSUTO
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 07-312585 [JP 95312585]
FILED: November 30, 1995 (19951130)
INTL CLASS: [6] G06F-012/00; G06F-005/00
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units); 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)
JAPIO KEYWORD: R131 (INFORMATION PROCESSING -- Microcomputers & Microprocessers)

ABSTRACT

PROBLEM TO BE SOLVED: To store and transfer program code or data with high efficiency by converting source data to a standard processor format.
SOLUTION: The block diagram of a standard processor data format encoder consists of five functional blocks, i.e., a **header** generating circuit 11,

a source data **file** [redacted]ser 12, a dual-buffer bank 13, [redacted]pack coded word connector and **byte** **swapper** 14, and a bit stream formatter 15. The functional block 14 packs each pack data word in specific format according to an Endian flag mark. Further, the bit stream formatter compose and [illegible] the **header** and pack coded word generated by the functional block 14 in the standard processor data format. Thus, the source data is converted to the standard processor format for storing and transmitting the processor program code and data.

11/5/5 **(Item 5 from file: 347)**
DIALOG(R)File 347:JAPIO
(c) 2004 JPO & JAPIO. All rts. reserv.

05247146 **Image available**
INPUT AND OUTPUT CONTROLLER

PUB. NO.: 08-202646 [JP 8202646 A]
PUBLISHED: August 09, 1996 (19960809)
INVENTOR(s): NISHIKAWA SATOSHI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 07-009374 [JP 959374]
FILED: January 25, 1995 (19950125)
INTL CLASS: [6] G06F-013/12; G06F-013/36
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units)

ABSTRACT

PURPOSE: To attain the software designing with giving no consideration to the Endian system of every input/output(I/O) device by easily connecting the I/O devices of different Endian systems to the same system.

CONSTITUTION: A comparator 12 of an I/O controller 1 retrieves an I/O address to be hit based on the I/O address latched by an address latch circuit 10 and also by referring to the address field of an **Endian** **conversion** **table** 13. The **table** 13 sends the **Endian** attribute corresponding to the retrieved I/O address to an **Endian** **converter** 14. The **converter** 14 applies the **Endian** **conversion** to the data latched by a data latch circuit 11 in response to the Endian attribute sent from the **table** 13. The data subjected to the data swap or data through are inputted to the I/O devices 2 and 3 via an I/O bus 110.

11/5/6 **(Item 6 from file: 347)**
DIALOG(R)File 347:JAPIO
(c) 2004 JPO & JAPIO. All rts. reserv.

05027064 **Image available**
SIGNAL PROCESSOR

PUB. NO.: 07-319664 [JP 7319664 A]
PUBLISHED: December 08, 1995 (19951208)
INVENTOR(s): KONDO HIROSHI
APPLICANT(s): CANON INC [000100] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-111023 [JP 94111023]
FILED: May 25, 1994 (19940525)
INTL CLASS: [6] G06F-005/00; G06F-012/04; G11B-020/12; H04N-005/225
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units); 42.5 (ELECTRONICS -- Equipment); 44.6 (COMMUNICATION -- Television); 45.2 (INFORMATION PROCESSING -- Memory Units)
JAPIO KEYWORD: R098 (ELECTRONIC MATERIALS -- Charge Transfer Elements, CCD & BBD); R131 (INFORMATION PROCESSING -- Microcomputers & Microprocessers)

ABSTRACT

PURPOSE: To process data fast even when data in the same **file** format are processed by using computers having different kinds of CPUs by converting

the order of data whose [redacted]cess units are plural reference [redacted]nits.

CONSTITUTION: A signal processing CPU 13 after processing image data into a **file** and storing the data in a buffer memory 12 requests a signal processing CPU 9 to send byte information. The control CPU 9 having received the signal reads byte order information out of an EEPROM 10 and outputs it to the signal processing CPU 13. The signal processing CPU 13 outputs a **byte order** decision signal to a data **converter** 18. The data **converter** 18 outputs the input image data as they are when the signal is at a low level, but replaces the high-order and low-order bytes of 16-bit data and outputs them when the signal is at a high level. Consequently, the image data can be recorded on a memory card 20 in specified byte order.

11/5/7 **(Item 7 from file: 347)**
DIALOG(R)File 347:JAPIO
(c) 2004 JPO & JAPIO. All rts. reserv.

04927223 **Image available**
INFORMATION PROCESSOR

PUB. NO.: 07-219823 [JP 7219823 A]
PUBLISHED: August 18, 1995 (19950818)
INVENTOR(s): KATO HIDEKI
NONAKA NAOMICHI
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-014208 [JP 9414208]
FILED: February 08, 1994 (19940208)
INTL CLASS: [6] G06F-012/00; G06F-013/00
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units)

ABSTRACT

PURPOSE: To attain the sharing of a text **file** by having a client- **Endian table** in a main storage and carrying out the **Endian conversion** when an access request is received from a client.

CONSTITUTION: When a client is connected to a server, the routine of an Endian register means 12 operates on the server. The deciding result of the routine is sent back to the server and written into a **table** 11. Then the routine of a means 13 operates on the server when the client gives a write request to the server. The server and the type of the Endian of the client are read out of the **table** 11. Then the server is compared with the Endian of the client. If they are different from each other, an **Endian conversion** routine 15 is called out and the **Endian** of a **file** is **converted** . Finally the result of **conversion** is sent to an OS and then stored in a disk device 30. If the server is equal to the **Endian** , the **Endian conversion** is not carried out. Therefore all **files** are integrated into the Endian.

11/5/8 **(Item 8 from file: 347)**
DIALOG(R)File 347:JAPIO
(c) 2004 JPO & JAPIO. All rts. reserv.

01603137 **Image available**
METHOD FOR COMPARING DISPLAY KEY OF DECIMAL NUMBER

PUB. NO.: 60-081637 [JP 60081637 A]
PUBLISHED: May 09, 1985 (19850509)
INVENTOR(s): HONMA YOSHIO
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 58-191182 [JP 83191182]
FILED: October 12, 1983 (19831012)
INTL CLASS: [4] G06F-007/02
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)
JOURNAL: Section: P, Section No. 387, Vol. 09, No. 224, Pg. 51,

ABSTRACT

PURPOSE: To obtain a decimal number key comparing method capable of comparison of decimal number keys successively from the leading byte similarly to binary numbers by displaying the code of the low-order bit of the least significant **byte** by the high- **order** bit of the most significant byte as a code, and **converting** a negative number into its complement to display it.

CONSTITUTION: A key number to be compared and retrieved is inputted to a retrieving part 1, which retrieves a **file** 5 and takes out the corresponding address. The retrieving part 1 discriminates the code of the input key and that of the address to determine the size of the codes and then a comparing part 3 compares the code of the input key with the high-order bit. The comparing part 3 actuates a shifting part 4 in accordance with compared result and the retrieving part 1 retrieves the **file** 5 by shifting the retrieving position right or left in accordance with the compared size. Said process is repeated to retrieve the corresponding key.

11/5/9 **(Item 1 from file: 350)**
DIALOG(R)File 350:Derwent WPIX
(c) 2004 Thomson Derwent. All rts. reserv.

015482563 **Image available**
WPI Acc No: 2003-544710/200352
XRPX Acc No: N03-432263
Information processor calls Endian conversion **routine when type of server and** Endian **of client differ and stores** converted Endian **of** file **in disk**
Patent Assignee: HITACHI LTD (HITA)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 7219823	A	19950818	JP 9414208	A	19940208	200352	B

Priority Applications (No Type Date): JP 9414208 A 19940208
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 7219823	A		6	G06F-012/00	

Abstract (Basic): JP 7219823 A
NOVELTY - A comparison unit compares type of server with type of **Endian** of client. An **Endian conversion** routine (15) is called out when the type of server and the **Endian** of client differ, to **convert Endian** of a **file** . The **converted file** is stored in a disk (30).
USE - Information processor.
ADVANTAGE - Enables to share the text **file** easily.
DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the information processor. (Drawing includes non-English language text).
table (11)
Endian conversion routine (15)
disk (30)
pp; 6 DwgNo 1/1
Title Terms: INFORMATION; PROCESSOR; CALL; CONVERT; ROUTINE; TYPE; SERVE; CLIENT; DIFFER; STORAGE; CONVERT; **FILE** ; DISC
Derwent Class: T01
International Patent Class (Main): G06F-012/00
International Patent Class (Additional): G06F-013/00
File Segment: EPI

11/5/10 **(Item 2 from file: 350)**
DIALOG(R)File 350:Derwent WPIX
(c) 2004 Thomson Derwent. All rts. reserv.

Image available
WPI Acc No: 2003-165869/200316
XRPX Acc No: N03-130975

Computerized data securing method involves using output of dynamic wave functions to alter numerical data such as computer byte values, for encrypting and decrypting data

Patent Assignee: SMITH S (SMIT-I)
Inventor: SMITH S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020146126	A1	20021010	US 2001279183	P	20010327	200316	B
			US 2002106340	A	20020326		

Priority Applications (No Type Date): US 2001279183 P 20010327; US 2002106340 A 20020326
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020146126	A1		7	H04K-001/00	Provisional application US 2001279183

Abstract (Basic): US 20020146126 A1

NOVELTY - The method involves using output of dynamic wave function or other similar functions to **alter** numerical data such as computer **byte** values, in **order** to encrypt and decrypt data.

USE - For securing computerized data contained in **files** and documents such as expense reports, etc.

ADVANTAGE - By using the dynamic wave functions, security of transmission of computerized data is improved.

DESCRIPTION OF DRAWING(S) - The figure shows the schematic illustration of the contents of the crypto-text **file** .

pp; 7 DwgNo 6/6

Title Terms: COMPUTER; DATA; SECURE; METHOD; OUTPUT; DYNAMIC; WAVE; FUNCTION; ALTER; NUMERIC; DATA; COMPUTER; BYTE; VALUE; DATA
Derwent Class: T01; W01; W02
International Patent Class (Main): H04K-001/00
File Segment: EPI

11/5/11 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004 Thomson Derwent. All rts. reserv.

014580980
WPI Acc No: 2002-401684/200243
XRPX Acc No: N02-314841

A pre-interpretation and execution method of a Java computer programming language - for the pre-interpretation and execution method for a Java programming language in OS of embedded equipment linked with network

Patent Assignee: INST INFORMATION IND (INFO-N)
Inventor: JOU W
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
TW 451154	A	20010821	TW 98111706	A	19980717	200243	B

Priority Applications (No Type Date): TW 98111706 A 19980717
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
TW 451154	A			G06F-009/45	

Abstract (Basic): TW 451154 A

NOVELTY - The invention relates to a pre-interpretation and execution method of a computer programming language, which is applied to the execution of the Java computer programming language in the OS of an embedded equipment in connection with a network. The method includes the following procedures: (a) establish a mapping **table** mapping the byte code execution code to the pointer of entry point for the

corresponding subrou[redacted]e in the embedded equipment; ([redacted]when downloading a Java program of the network of the embedded equipment, **orderly convert** each received **byte** code execution code in accordance with the mapping **table** to the pointer data of the entry point in the corresponding subroutine, and convert the arithmetic units from networking format to machine format to store them in sequence to the embedded equipment after going through the adjustment procedures for maintaining the correctness of its relative address; and (c) orderly read the pointer data representing the corresponding subroutine and operands in machine format and execute to finish the execution of the Java program in the OS of the embedded equipment.

DwgNo 0/1

Title Terms: PRE; INTERPRETATION; EXECUTE; METHOD; COMPUTER; PROGRAM; LANGUAGE; PRE; INTERPRETATION; EXECUTE; METHOD; PROGRAM; LANGUAGE; OS; EMBED; EQUIPMENT; LINK; NETWORK
Derwent Class: T01
International Patent Class (Main): G06F-009/45
File Segment: EPI

11/5/12 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004 Thomson Derwent. All rts. reserv.

014501767 **Image available**
WPI Acc No: 2002-322470/200236
XRPX Acc No: N02-252866
Data converter for common key block encryption system, changes higher and lower order bytes of input data in each stage, depending on page number
Patent Assignee: NIPPON TELEGRAPH & TELEPHONE CORP (NITE)
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2002023621	A	20020123	JP 2000211244	A	20000712	200236	B
JP 3492988	B2	20040203	JP 2000211244	A	20000712	200410	

Priority Applications (No Type Date): JP 2000211244 A 20000712
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2002023621	A		13	G09C-001/00	
JP 3492988	B2		11	G09C-001/00	Previous Publ. patent JP 2002023621

Abstract (Basic): JP 2002023621 A

NOVELTY - The values of data (X1-X4) containing four bytes (a-d,e-h,i-l,m-p) respectively, are determined with reference to a **table** (SPno). Higher and lower order bytes of respective inputs (X1,X2) are interchanged and is output as X3, X4 in the following stages. The higher and lower **order bytes** in each successive stages, are **changed** depending on number of pages.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) Data conversion method;

(b) Recorded medium storing data conversion program

USE - For common key block encryption system.

ADVANTAGE - A memory capacity of a **table** is reduced, thereby high speed data conversion is enabled.

DESCRIPTION OF DRAWING(S) - The figure shows the data converter.

(Drawing includes non-English language text).

pp; 13 DwgNo 1/12

Title Terms: DATA; CONVERTER; COMMON; KEY; BLOCK; ENCRYPTION; SYSTEM; CHANGE; HIGH; LOWER; ORDER; BYTE; INPUT; DATA; STAGE; DEPEND; PAGE; NUMBER
Derwent Class: P85; T01
International Patent Class (Main): G09C-001/00
File Segment: EPI; EngPI

11/5/13 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004 Thomson Derwent. All rts. reserv.

0136 9478 **Image available**
WPI Acc No: 2001-093686/200111
Related WPI Acc No: 2001-104665
XRPX Acc No: N01-071078
Apparatus for preprocessing of data packets in a bus interface unit by byte order change of header quadlets of the asynchronous data packets in a data link layer unit
Patent Assignee: DEUT THOMSON-BRANDT GMBH (THOH)
Inventor: BRUNE T; CAHNBLEY J; OSTERMANN R; SCHWEIDLER S
Number of Countries: 028 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1058193	A1	20001206	EP 99110490	A	19990531	200111	B
JP 2001016230	A	20010119	JP 2000160806	A	20000530	200120	
CN 1284673	A	20010221	CN 2000109307	A	20000529	200131	
KR 2001014980	A	20010226	KR 200029101	A	20000529	200156	

Priority Applications (No Type Date): EP 99110490 A 19990531; EP 2000250024 A 20000126
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1058193	A1	E	14	G06F-013/40	
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI					
JP 2001016230	A		11	H04L-012/28	
CN 1284673	A			G06F-013/40	
KR 2001014980	A			H04L-012/40	

Abstract (Basic): EP 1058193 A1
NOVELTY - A quadlet (25) is shown of asynchronous **header** data for which byte reordering is being made and reordering is carried out directly after receiving the 1394 packet. The application data receives quadlets (27) in right **byte order** and wrong results are avoided during evaluation. The order **change** is carried out so that a data processor (30) can interpret the data word order and reordering is carried out automatically in the link layer unit in the multiplexing device (24) under control of a little endian flag (23) in a status register (22).
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for a method of preprocessing data packets and for a bus interface unit.
USE - Preprocessing data packets received via a communication bus.
ADVANTAGE - No requirement for processing power of the application data processing unit for byte reordering.
DESCRIPTION OF DRAWING(S) - The drawing illustrates **byte order change** in a data link layer
Quadlets (25,27)
Multiplexing device (24)
Data processor (30)
Endian flag (23)
Status register (22)
pp; 14 DwgNo 5/6
Title Terms: APPARATUS; DATA; PACKET; BUS; INTERFACE; UNIT; BYTE; ORDER; CHANGE; **HEADER** ; ASYNCHRONOUS; DATA; PACKET; DATA; LINK; LAYER; UNIT
Derwent Class: T01; W01
International Patent Class (Main): G06F-013/40; H04L-012/28; H04L-012/40
International Patent Class (Additional): G06F-013/12; H04L-029/06
File Segment: EPI

11/5/14 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004 Thomson Derwent. All rts. reserv.

013461631 **Image available**

WPI Acc No: 2000-633574/[redacted]061
XRPX Acc No: N00-469593
Code converting system has memory with code conversion table to store lower order code for certain time when odd number is input
Patent Assignee: NEC CORP (NIDE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2000259613	A	20000922	JP 9967040	A	19990312	200061	B

Priority Applications (No Type Date): JP 9967040 A 19990312
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2000259613	A		7	G06F-017/21	

Abstract (Basic): JP 2000259613 A

NOVELTY - A data converter (2) converts code of input data. A memory (3) has code **conversion tables** (31,32) for storing higher order code and lower **order** code of one **byte** , before and after **conversion** of two byte character code. Another code conversion **table** (33) stores lower order code for certain time when odd number is entered.

USE - Code converting system.

ADVANTAGE - Code conversion is performed at high speed.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of code converting system.

Data converter (2)

Memory (3)

Code conversion **tables** (31-33)

pp; 7 DwgNo 1/5

Title Terms: CODE; CONVERT; SYSTEM; MEMORY; CODE; CONVERT; **TABLE** ; STORAGE ; LOWER; ORDER; CODE; TIME; ODD; NUMBER; INPUT
Derwent Class: T01
International Patent Class (Main): G06F-017/21
File Segment: EPI

11/5/15 **(Item 7 from file: 350)**
DIALOG(R)File 350:Derwent WPIX
(c) 2004 Thomson Derwent. All rts. reserv.

013176384
WPI Acc No: 2000-348257/200030
XRPX Acc No: N00-260824
Gathering of performance traces from platforms with different endianess in an operating system ported to multiple hardware platforms
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
RD 431122	A	20000310	RD 2000431122	A	20000220	200030	B

Priority Applications (No Type Date): RD 2000431122 A 20000220
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
RD 431122	A		1	G06F-000/00	

Abstract (Basic): RD 431122 A

NOVELTY - A better solution for collecting performance traces is to let the processor write the trace data with its inherent endianess, to put an endianess identification field in the trace **header** and to handle the endianess issue during post processing. A known value in hex is written as a 32 bit int by the processor into the trace **header** and the trace data consist of individual hook writes, each hook containing various fields which can be numeric and/or string data. All numeric fields go through an additional step during post processing for **conversion** into a desired **endian** order.

USE - Abstraction of endianess in a trace collector from platforms.

pp; 1 DwgNo 0/0
Title Terms: GATHER; PERFORMANCE; TRACE; PLATFORM; OPERATE; SYSTEM; PORT; MULTIPLE; HARDWARE; PLATFORM
Derwent Class: T01
International Patent Class (Main): G06F-000/00
File Segment: EPI

11/5/16 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004 Thomson Derwent. All rts. reserv.

011804800 **Image available**
WPI Acc No: 1998-221710/199820
XRPX Acc No: N98-175567
Mirror conversion system for 16-bit data used in e.g. mobile communication - has second mirror converter which receives mirror output of operation unit corresponding to value of lower order byte data extracted from mirror conversion table
Patent Assignee: NIPPON DENKI IDO TSUSHIN KK (NIDE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 10063475	A	19980306	JP 96214818	A	19960814	199820	B

Priority Applications (No Type Date): JP 96214818 A 19960814
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 10063475	A		6	G06F-005/00	

Abstract (Basic): JP 10063475 A
The system consists of a first mirror converter (2) which receives 16-bit data for mirror **conversion** . The mirror **conversion** of the low **order byte** of the 16-bit data is performed.
An operation unit (3) interchanges the higher **order byte** and the lower **order byte** of the 16-bit data output by the mirror **convertor** . A second mirror convertor (4) receives the output of the operation unit corresponding to the value of the lower **order byte** data extracted from a mirror **conversion table** (6).
ADVANTAGE - Enables to perform mirror conversion of 16-bit data easily.
Dwg.1/7
Title Terms: MIRROR; CONVERT; SYSTEM; BIT; DATA; MOBILE; COMMUNICATE; SECOND; MIRROR; CONVERTER; RECEIVE; MIRROR; OUTPUT; OPERATE; UNIT; CORRESPOND; VALUE; LOWER; ORDER; BYTE; DATA; EXTRACT; MIRROR; CONVERT; **TABLE**
Derwent Class: T01
International Patent Class (Main): G06F-005/00
File Segment: EPI

11/5/17 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004 Thomson Derwent. All rts. reserv.

010623713 **Image available**
WPI Acc No: 1996-120666/199613
XRPX Acc No: N96-101109
Code converter for word processor or computer - has character code output unit which outputs arithmetic sum of first conversion code information and second conversion code
Patent Assignee: FUJI XEROX CO LTD (XERF)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 8016360	A	19960119	JP 94151839	A	19940704	199613	B

Priority Applications (No Type Date): JP 94151839 A 19940
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
JP 8016360 A 8 G06F-005/00

Abstract (Basic): JP 8016360 A
The code converter has a memory which stores a first conversion **table** and a second conversion **table** . A first read-out unit reads a first character attribute information, a first conversion code information and a **conversion table** specification information corresponding to the higher- **order byte** of the input character code from the first **conversion table** .
A second read-out unit reads a second character attribute information and a second conversion code information from the second **conversion table** corresponding to the lower- **order byte** of the input character code. A character code output unit outputs an arithmetic sum of the first conversion code and the second conversion code. The logical product of the first and the second character attribute information is also output.
ADVANTAGE - Reduces amount of storage capacity needed.
Dwg.1/6
Title Terms: CODE; CONVERTER; WORD; PROCESSOR; COMPUTER; CHARACTER; CODE; OUTPUT; UNIT; OUTPUT; ARITHMETIC; SUM; FIRST; CONVERT; CODE; INFORMATION; SECOND; CONVERT; CODE
Derwent Class: T01; U21
International Patent Class (Main): G06F-005/00
International Patent Class (Additional): G06F-003/12; G06F-017/21
File Segment: EPI

11/5/18 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004 Thomson Derwent. All rts. reserv.

009697493 **Image available**
WPI Acc No: 1993-391046/199349
XRPX Acc No: N93-302351
Data byte order alteration **device - has order conversion** table **for converting data, conversion** table **read-out unit corresp. to communication party and order** alteration **unit to enable transmission of data in** converted byte order **NoAbstract**
Patent Assignee: MITSUBISHI HEAVY IND CO LTD (MITO)
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
JP 5292144 A 19931105 JP 9284286 A 19920407 199349 B

Priority Applications (No Type Date): JP 9284286 A 19920407
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
JP 5292144 A 4 H04L-029/06

Abstract (Basic): JP 5292144 A
Dwg.1/3
Title Terms: DATA; BYTE; ORDER; ALTER; DEVICE; ORDER; CONVERT; **TABLE** ; CONVERT; DATA; CONVERT; **TABLE** ; READ-OUT; UNIT; CORRESPOND; COMMUNICATE; PARTY; ORDER; ALTER; UNIT; ENABLE; TRANSMISSION; DATA; CONVERT; BYTE; ORDER; NOABSTRACT
Derwent Class: W01
International Patent Class (Main): H04L-029/06
International Patent Class (Additional): H04L-012/28
File Segment: EPI

11/5/19 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004 Thomson Derwent. All rts. reserv.

007803884 **Image ava[redacted]ble**
WPI Acc No: 1989-068996/198909
XRPX Acc No: N89-052604

Input-output module control system - is used for data transfer of I-O modules used for programmable machine controller

Patent Assignee: FANUC LTD (FUFA)
Inventor: CHIBA K; TANAKA K

Number of Countries: 004 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 8901666	A	19890223	WO 88JP790	A	19880810	198909	B

Priority Applications (No Type Date): JP 87201598 A 19870812
Cited Patents: AU 8310735; BR 8300365; CA 1184311; JP 53080932; JP 57185536 ; JP 58134324; JP 60138664; JP 62154049; US 4509113
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 8901666	A	J	13		

Designated States (National): US
Designated States (Regional): DE FR GB

Abstract (Basic): WO 8901666 A

Data for interchanging high- **order bytes** and low- **order bytes** are included in an allocating **table** (5a) to **convert** the word structure for data transfer from the I/O modules (6,7) to the RAM (4). Since high-order bytes and low-order bytes are interchanged any I/O module designed for the word structure adapted for one processor can be directly coupled to a system that is constituted using another processor.

16/5/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2004 JPO & JAPIO. All rts. reserv.

06788749 **Image available**
PRE-PROCESSING METHOD FOR DATA PACKET RECEIVED VIA COMMUNICATION BUS BY BUS INTERFACE UNIT, THE BUS INTERFACE UNIT AND APPLICATION DATA PROCESSING UNIT

PUB. NO.: 2001-016230 [JP 2001016230 A]
PUBLISHED: January 19, 2001 (20010119)
INVENTOR(s): BRUNE THOMAS
OSTERMANN RALF
CAHNBLEY JENS
SCHWEIDLER SIEGFRIED
APPLICANT(s): DEUTSCHE THOMSON BRANDT GMBH
APPL. NO.: 2000-160806 [JP 2000160806]
FILED: May 30, 2000 (20000530)
PRIORITY: 99110490 [EP 99110490], EP (European Patent Office), May 31, 1999 (19990531)
00250024 [EP 2000250024], EP (European Patent Office), January 26, 2000 (20000126)
INTL CLASS: H04L-012/28; G06F-013/12

ABSTRACT

PROBLEM TO BE SOLVED: To simply configure a multiplexer to rearrange byte sequence not by changing the byte sequence in a **header** data field but by changing the byte sequence in a payload data field.

SOLUTION: The byte sequence in a **header** data field is not changed but the byte sequence in a payload data field is changed. A data link layer unit 21 automatically rearranges the byte sequence of an asynchronous data packet by means of the hardware. A corresponding multiplexer 24 rearranges the byte sequence under the control of a little **endian** flag 23. This flag is set while a data link layer IC 21 is initialized. This IC 21 is initialized after interruption of power by using a specific program working on an application processing unit 30.

COPYRIGHT: (C)2001,JPO

16/5/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004 Thomson Derwent. All rts. reserv.

013620457
WPI Acc No: 2001-104665/200112
Related WPI Acc No: 2001-093686
XRPX Acc No: N01-077624
Method of pre-processing data packets received over a bus in which the packets include a payload field and a multi-byte header **field and the bytes are re-ordered depending on whether the destination is of big or little** endian **type**
Patent Assignee: DEUT THOMSON-BRANDT GMBH (THOH); THOMSON LICENSING SA (CSFC)
Inventor: BRUNE T; CAHNBLEY J; OSTERMANN R; SCHWEIDLER S
Number of Countries: 029 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1059590	A1	20001213	EP 2000110251	A	20000519	200112	B
JP 2001016230	A	20010119	JP 2000160806	A	20000530	200120	
CN 1284673	A	20010221	CN 2000109307	A	20000529	200131	
KR 2001014980	A	20010226	KR 200029101	A	20000529	200156	
US 6622187	B1	20030916	US 2000583056	A	20000530	200362	

Priority Applications (No Type Date): EP 2000250024 A 20000126; EP 99110490 A 19990531
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes

EP 1059590 A1 E 16 G[redacted]-013/40
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
JP 2001016230 A 11 H04L-012/28
CN 1284673 A G06F-013/40
KR 2001014980 A H04L-012/40
US 6622187 B1 G06F-013/00

Abstract (Basic): EP 1059590 A1

NOVELTY - The IEEE1394 bus protocol has three layers, including a physical layer, a link layer and a transaction layer. The **header** data of each asynchronous data packet is ordered either in big **endian** form with the most significant byte is stored in the lowest address, or in little **endian** form with the least significant byte stored in the lowest address. Depending on the requirements of an application data processor which is to receive the data, the bytes are re-ordered depending on whether the destination operates as a big or little **endian** . The re-ordering is done in hardware in the link layer of the bus interface. Either the **header** data or the payload data is re-ordered.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for
(a) a bus interface unit
(b) and an application data processor.

USE - In a data processing network.

ADVANTAGE - No processing is required to re-order the data in the application data processor.

pp; 16 DwgNo 0/7

Title Terms: METHOD; PRE; PROCESS; DATA; PACKET; RECEIVE; BUS; PACKET; PAYLOAD; FIELD; MULTI; BYTE; **HEADER** ; FIELD; BYTE; ORDER; DEPEND; DESTINATION; BIG; TYPE
Derwent Class: T01; W01
International Patent Class (Main): G06F-013/00; G06F-013/40; H04L-012/28; H04L-012/40
International Patent Class (Additional): G06F-013/12; G06F-013/14; H04L-029/06
File Segment: EPI

16/5/3 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004 Thomson Derwent. All rts. reserv.

012140066 **Image available**
WPI Acc No: 1998-556978/199847
XRPX Acc No: N98-434232

Computer readable storage medium for data processing system - stores objects which contain information relating to their size and function and are shared among various applications

Patent Assignee: APPLE COMPUTER INC (APPY)
Inventor: TURKOWSKI K E
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5819283	A	19981006	US 9362620	A	19930511	199847	B
			US 97911347	A	19970814		

Priority Applications (No Type Date): US 9362620 A 19930511; US 97911347 A 19970814
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5819283	A		12	G06F-017/30	Cont of application US 9362620

Abstract (Basic): US 5819283 A

The medium includes a **header** (29) comprising identifier (X0-X3), version number (X4), revision number (X5), **endian** code (X6) and a reserved byte (X7) respectively.

The objects (33) are shared among various applications programs stored in program memory (23). These objects contain information

relating to their size and function.

ADVANTAGE - Simplifies data structure. Allows objects to be shared by several computer applications.

Dwg.2a,2b/

```
File 348:EUROPEAN PATENT(  )978-2004/Jun W02
         (c) 2004 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20040610,UT=20040603
         (c) 2004 WIPO/Univentio

Set     Items   Description
S1        490   (ENDIAN? OR (ORDER??? OR ARRANG?)(3N)BYTE? ?)(10N)(CONVERT?
                OR CONVERSION OR TRANSFORM? OR TRANSLAT? OR CHANG??? OR EXCH-
                ANG??? OR SWITCH??? OR SWAP???? OR MODIF???? OR MODIFICATION?
                ? OR ALTER??? OR ALTERATION? ? OR FLIP????)
S2        439   BYTE? ?(5N)(SWAP???? OR REORDER? OR RE()ORDER??? OR INTERC-
                HANG???)
S3      40744   HEADER? ?
S4      25313   LUT OR LUTS OR (LOOKUP OR LOOK()UP)()TABLE? ?
S5     154404   FILE? ?(5N)ACCESS??? OR FILESYSTEM? ? OR FILE()SYSTEM? ? OR
                FAT?? OR NTFS
S6         41   S1:S2(50N)S3
S7         18   S1:S2(50N)S4:S5
S8         57   S6:S7
S9        710   ENDIAN?
S10        87   S9(50N)S3:S5
S11        73   S10 NOT S8
S12         4   S9(100N)(FILE? ?(5N)ACCESS???)
S13         3   S12 NOT S8
```

8/3,K/43 (Item 21 f[redacted] file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2004 WIPO/Univentio. All rts. reserv.

00560529 **Image available**
DYNAMIC CONVERSION OF BYTE ORDERING FOR USE ON DIFFERENT PROCESSOR PLATFORMS
CONVERSION DYNAMIQUE D'ORDONNANCEMENT DE MULTIPLETS DESTINEE A ETRE UTILISEE SUR DIFFERENTES PLATES-FORMES DE PROCESSEUR
Patent Applicant/Assignee:
SOFTBOOK PRESS INC,
Inventor(s):
DUGA Brady,
MARDER Andrew,
CONBOY Garth,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200023902 A1 20000427 (WO 0023902)
Application: WO 99US23542 19991008 (PCT/WO US9923542)
Priority Application: US 98174072 19981016
Designated States: AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW GH GM KE LS MW SD SL SZ TZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
Publication Language: English
Fulltext Word Count: 3065

Fulltext Availability:
Claims

Claim
... start of a short counted list, a start of a long counted list, and an end of a counted list.

7 A system for dynamically **converting byte - ordering** of a data structure of a resource type from a first format to a second format, the first format being incompatible with the second format, the system comprising:
(a) a server including:
a resource **file system** having a database for storing the resource type, the resource type being stored in a first format, the resource file system creating a template corresponding...

8/3,K/44 (Item 22 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2004 WIPO/Univentio. All rts. reserv.

00551552
METHOD AND SYSTEM FOR THE PROTECTED DISTRIBUTION OF NETWORK FILES
PROCEDE ET SYSTEME DE REPARTITION PROTEGEE DE FICHIERS DE RESEAU
Patent Applicant/Assignee:
MUSICMARC INC,
HAHN Yehuda,
Inventor(s):
HAHN Yehuda,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200014925 A2 20000316 (WO 0014925)
Application: WO 99IL497 19990909 (PCT/WO IL9900497)
Priority Application: IL 126147 19980909
Designated States: AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZA ZW GH GM KE LS MW SD SL SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
Publication Language: English

Fulltext Word Count: 306
Fulltext Availability:
  Detailed Description

Detailed Description
... literal.

  Parameters.

  (WORD): Input WORD.

  Return.

  (BYTE): Output BYTE.

  (BYTE): Input BYTE.

  Return.

  (WORD): Output WORD.

  void CRSHTTPRESPONSE::InitConvTable(void);
  This function initializes the byteToWord **lookup table** .
  LPSTR CRSHTTPRESPONSE::ConvertToString(void);
  This function converts the CRSHTTPRESPONSE data to a portable 7-bit text unescaped string representation. The string is 115 bytes long and consists of a three byte **header** followed by a 56 WORD representation of the byte pattern of the CRSHTTPRESPONSE in little- **endian** unpadded order, **converted** using byteToWord.

  The first three letters are "ACK", which are all illegal bytes in the byteToWord conversion algorithm.

  ConvertToString also updates the NM5 localsign member...

 8/3,K/45 **(Item 23 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT
(c) 2004 WIPO/Univentio. All rts. reserv.

WO 2296 **Image available**
SYSTEM AND PROCESS FOR HIGH-SPEED PATTERN MATCHING FOR APPLICATION-LEVEL SWITCHING OF DATA PACKETS
SYSTEME ET PROCEDE DE CORRELATION DES CONFIGURATIONS HAUTE VITESSE POUR LA COMMUTATION A NIVEAU D'APPLICATION DE PAQUETS DE DONNEES
Patent Applicant/Assignee:
  TOP LAYER NETWORKS INC,
Inventor(s):
  ROBINS Cary B,
  NARAYANASWAMY Krishna,
  ROSS Theodore L,
  SPINNEY Barry A,
Patent and Priority Information (Country, Number, Date):
  Patent: WO 9953648 A2 19991021
  Application: WO 99US7808 19990409 (PCT/WO US9907808)
  Priority Application: US 9858597 19980410
Designated States: AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZA ZW GH GM KE LS MW SD SL SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
Publication Language: English
Fulltext Word Count: 18291

Fulltext Availability:
  Claims

Claim
... time.

6 A method for identifying, retrieving and sending the flow path switching information of a packet of information comprising the steps of:
retrieving the **header** of the packet;
selecting relevant bytes in the **header** ;
forming an ordered set of said selected **bytes** ;
hashing the **ordered** set first to form a hash result and,
with **changed** hashing parameters to form a signature result;
selecting portions of the hash result to form an index into a memory;
retrieving a valid flow tag...

8/3,K/46 (Item 24 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2004 WIPO/Univentio. All rts. reserv.

00484848 **Image available**
INTELLIGENT DATA BUS INTERFACE USING MULTI-PORT MEMORY
INTERFACE DE BUS DE DONNEES INTELLIGENTE DANS LAQUELLE UNE MEMOIRE A ACCES MULTIPLES EST UTILISEE
Patent Applicant/Assignee:
ICORE TECHNOLOGIES INC,
Inventor(s):
LINDENSTRUTH Volker,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9916200 A2 19990401
Application: WO 98US20049 19980922 (PCT/WO US9820049)
Priority Application: US 97935921 19970923
Designated States: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH HU IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW GH GM KE LS MW SD SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
Publication Language: English
Fulltext Word Count: 9309
Fulltext Availability:
Detailed Description

Detailed Description
... order for the pass-through-logic device 80 to accept and forward the request to the PCI interface 68.

The upper two bits from the **look - up table** define a 2-bit control field 1 1 6. The first bit of the control field 1 16 is used as a write protect bit and the second bit is used to control a **byte swap** engine of the PCI interface 68. This feature allows a page by - 25 page **endianess conversion** . The remaining fourteen bits from the **lookup table** form bits 16 through 29 of the PCI master address. The upper two PCI address bits are defined by a CSR register and define the PCI master base address. This grants a 1 GB PCI address window. The SCI-to-PCI **LUT** can be any memory size. If 512 address translation entries are not sufficient, a larger memory can be used, allowing a larger LUT index 112 ...

8/3,K/47 (Item 25 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2004 WIPO/Univentio. All rts. reserv.

00448298
DETERMINING VISIBILITY TO A REMOTE DATABASE CLIENT
PROCEDE VISANT A DETERMINER, AU PROFIT D'UN TELE-CLIENT DE BASE DE DONNEES, LA VISIBILITE D'UNE PLURALITE DE TRANSACTIONS DE BASES DE DONNEES PAR

UTILISATION D'UN SER[redacted]R MANDATAIRE EN RESEAU

Patent Applicant/Assignee:
SIEBEL SYSTEMS INC,
ROTHWEIN Thomas Michael,
COKER John L,
Inventor(s):
ROTHWEIN Thomas Michael,
COKER John L,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9838762 A2 19980903
Application: WO 98US2756 19980224 (PCT/WO US9802756)
Priority Application: US 9739167 19970226
Designated States: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM GW HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZW GH GM KE LS MW SD SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN ML MR NE SN TD TG
Publication Language: English
Fulltext Word Count: 19422

Fulltext Availability:
Detailed Description

Detailed Description
... the NUL byte), although usually these will be true C strings which are NUL terminated. Strings are always byte-oriented since the data is not **byte swapped** for transmission.

The length of the **header** and the length of the body are both explicitly given.

This allows for advances in the protocol to be made without breaking older implementations (unless...

8/3,K/48 (Item 26 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2004 WIPO/Univentio. All rts. reserv.

00428773 **Image available**
USING A HIGH LEVEL PROGRAMMING LANGUAGE WITH A MICROCONTROLLER
UTILISATION DE LANGAGE DE PROGRAMMATION EVOLUE AVEC UN CONTROLEUR MICROPROGRAMME
Patent Applicant/Assignee:
SCHLUMBERGER TECHNOLOGIES INC,
Inventor(s):
WILKINSON Timothy J,
GUTHERY Scott B,
KRISHNA Ksheerabdhi,
MONTGOMERY Michael A,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9819237 A1 19980507
Application: WO 97US18999 19971022 (PCT/WO US9718999)
Priority Application: US 9629057 19961025
Designated States: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW GH KE LS MW SD SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN ML MR NE SN TD TG
Publication Language: English
Fulltext Word Count: 23003

Fulltext Availability:
Detailed Description

Detailed Description

... int
push(1) stkO<-ref
stkO==ref stkO<-int
DUPs, SWAP instructions
INVOKE instructions
FIELDS instructions
stkO<-ref
SUBSTITUTE SHEET (RULE 26)
... Standard Java **Byte** Code (without **reordering**) - Aftribute **Lookup Table**
Table of bytecode decode information. This contains a bytecode type and a bytecode length. We currently support all standard bytecodes (ie. no quicks) which gives...

8/3,K/49 (Item 27 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2004 WIPO/Univentio. All rts. reserv.

00415572 **Image available**
EMBEDDED WEB SERVER
SERVEUR WEB INTEGRE
Patent Applicant/Assignee:
AGRANAT SYSTEMS INC,
Inventor(s):
AGRANAT Ian D,
GIUSTI Kenneth A,
LAWRENCE Scott D,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9806033 A1 19980212
Application: WO 97US13817 19970808 (PCT/WO US9713817)
Priority Application: US 9623373 19960808
Designated States: JP AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Publication Language: English
Fulltext Word Count: 55647

Fulltext Availability:
Detailed Description

Detailed Description
... files forthe local Unix
development environment target. Typing "make" will build the EmWeb/Compiler, the example archives, and the reference Unix port.

4,11, Configuration **Header** Files
The sic/config/ew types. h file contains definitions for base 0 types used throughout the EmWeb/Server, Most of these are straightforward and generally do not require modification under 32-bit CPU architectures. The one definition which may require **modification** by the system integrator is the preprocessor symbol F.MwEB. **ENDIAN** which is defined to either EMWEB ENDIAN BIG or EMWEB EMIAN LITTLE, and reflects the byteorder of the target processor Cintel processors are@generally little...

8/3,K/50 (Item 28 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2004 WIPO/Univentio. All rts. reserv.

00410488 **Image available**
CENTRALIZED SECURE COMMUNICATIONS SYSTEM
SYSTEME DE COMMUNICATIONS DE SECURITE CENTRALISE
Patent Applicant/Assignee:
ALLSOFT DISTRIBUTING INC,
Inventor(s):
COLVIN Bryan Sr,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9800947 A1 19980108

Application: [redacted]97US11621 19970701 (PCT/WO US[redacted]1621)
Priority Application: US 96673122 19960701
Designated States: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES
FI GB GE GH HU IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN
MW MX NO NZ PL PT RO RU SD SE SG SI SK TJ TM TR TT UA UG UZ VN YU ZW GH
KE LS MW SD SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH DE DK ES FI FR
GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN ML MR NE SN TD TG
Publication Language: English
Fulltext Word Count: 13602

Fulltext Availability:
Detailed Description

Detailed Description

```
...  B = G-MAP I [G
  MAPO[A] I STATE[StatePointer] I PKEY[KeyPointer]];
  INC(;
  STATE[KeyPointer]A=PKEY[G-MAPO[StatePointer]];
  Method++;
  break;
  case 6:  LUT  #I
  B G-MAPO[G
  MAP I [A] I STATE[StatePointer] I PKEY[KeyPointer]],
  INC(;
  STATE[KeyPointer]"@=PKEY[GMAP I [KeyPointer]];
  Method=O;
  break;
  B A=Spin;
  Spin A= PKEY[KeyPointer]'STATE[Spin+ I
  ]]A=
  1 5 STATE [( byte )AlgorithmPointer[ I  SWAP (Spin,STATE[Spinj);
  STATE[( byte )AlgorithmPointer[2]]A=
   SWAP (Spin ASTATE[( byte )AlgorithmPointer[l]], STATE[StatePointer]);
  B'=G
  CopyRight[CopyPtr++]; // use copyright notice to mess up stuff'!
  CopyPtr&=Oxff;
  return B;
  byte CRYPT::SUM(byte A, byte...

...B = G
  MAPO[G
  MAP I [A] /I STATE[StatePointer] A PKEY[KeyPointer]];
  INC(;
  5 STATE[KeyPointer]'=PKEY[G
  MAPO'StatePointer]];
  Method++;
  break;
  case 6:  LUT  #I
  B G
  MAP1 [G
  MAPO[A] A STATE[StatePointer] I PKEY[KeyPointer]];
  INC(;
  STATE[KeyPointer]A =PKEY[G
  MAP I [KeyPointer]];
  Method=O;
  break;
  H each use of the AlgorithmPointer causes the algorithm to behave
  differently
  Spin l= PKEY[KeyPointerl'STATE[Spin+l];
  STATE[( byte )AlgorithmPointer[ I ]]A=  SWAP (Spin,STATE[Spin]);
  STATE[( byte )AlgorithmPointer[2]]A=
  3 0  SWAP (Spin'STATE[( byte )AlgorithmPointer[ I
  ]],STATE[StatePointer]);
  A=13ADataSpinZA DataSpinY; H undo data entered into random data stream.

  DataSpinY+=DataSpinZ;
  DataSpinZ'=A; H reverse data dependent encryption!
  return...
```

8/3,K/51 (Item 29 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2004 WIPO/Univentio. All rts. reserv.

00382333 **Image available**
SYSTEM AND METHOD FOR GENERAL PURPOSE NETWORK ANALYSIS
SYSTEME ET PROCEDE POUR L'ANALYSE DE RESEAU POLYVALENTE
Patent Applicant/Assignee:
N B NETWORKS,
Inventor(s):
BAKER Peter D,
NEAL Karen,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9723076 A1 19970626
Application: WO 96US20779 19961213 (PCT/WO US9620779)
Priority Application: US 95575506 19951220
Designated States: AU CA CN IL JP MX SG AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Publication Language: English
Fulltext Word Count: 39847

Fulltext Availability:
Detailed Description

Detailed Description
... right shift 32
14 ffmt number indicating a display type (i.e., decimal, hi!x,
15 flflag flag indicating value is actual length of protocol **header** (multiplier)
16 reserved not used ... pad byte to align following fields
17 fmult multiplier to apply to value prior to display
18 fswap flag indicating the need to **swap** **bytes** and words in 32 bit field containing value
19 fsdspfield flag indicating that this field should be displayed
20-23 fname pointer to field name...right shift of the '32-bit
[illegible],
the number indicating the display type,
the flag indicating the value is the actual length of
the protocol **header** ,
the reserved byte,
the multiplier to apply to value prior to display,
the flag indicating whether to **byte** **swap** the 32-bit value
the flag indicating that the field is ---o be displayed,
the length of the field name including thE! NULL terminator, or...en, Parsel-en, ProtoParseLen, HeaderLen;
U32 Srclntf = 0, IntfTypes[2561 = {ETHERNET, FDDI, TOKEN RING);
RouteTableEntry *RtePtr;
Filters CfgFilters; 11 Configured Filters Object
1 5
/I **Lookup** **table** for bit- **swapping** a **byte** value
S8 bs[2561 11 Table to perform bit-swapping
2 0
OxBO,Ox8O,Ox4O,OxcO,Ox2O,OxaO,Ox6O,OxeO,Ox1D,Dx9O,Ox5O,OxdO,Ox3O...
verify({ return(O); I/ Verify checksum
virtual void compute(J/ Compute checksum
0
It Derived Class definition verifying and computing IP Checksurns
I/ Verify IP **Header** Checksum in Network **Byte** **Order** ... No **byte** **swapping** required
11 (Assumes **Header** Length is greater than 4 32-bit words)
'. (Returns 0 if checksum OK, non-zero otherwise)
extern U32 ChklpCsum(S8 I); I/ Clocks = 14...0.360 usecs; 60 --- 0.660 usecs)

U16 *csum = 016 *)Pars[redacted] + 5); 11 Declare Pointer to [redacted]cksum Field
*csum = 0; 11 Clear Checksum in IP **Header**
*csum = (U16)ChklpCsum(ParsePtr); I/ Compute and Update Checksum
1S private.

I/ Derived Class definition verifying and computing IPX Checksurns
J/ Verify IPX **Header** Checksum in Network **Byte Order** ... No **byte swapping** required 11 (Assumes Checksum Field is NOT Oxffff, and 30 > = Length Field < Oxffff)
/I (Returns 0 if checksum OK, non-zero otherwise)
extern U32 ChklpxCsum...

8/3,K/52 (Item 30 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2004 WIPO/Univentio. All rts. reserv.

00363201 **Image available**
TELECOMMUNICATIONS APPARATUS AND METHOD
APPAREIL ET PROCEDE DE TELECOMMUNICATIONS
Patent Applicant/Assignee:
NORTHERN TELECOM LIMITED,
Inventor(s):
IRWIN George Frank,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9703526 A2 19970130
Application: WO 96CA430 19960626 (PCT/WO CA9600430)
Priority Application: US 95938 19950707; US 96655402 19960530
Designated States: CA CN JP KR AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Publication Language: English
Fulltext Word Count: 31761

Fulltext Availability:
Detailed Description

Detailed Description
... stream and
- 14
transferring the data packet payloads in the order of selection into an outgoing data stream;
in response to the timeslot switching information, **reordering** the **bytes** of a payload of synchronous data in the outgoing data stream, whereby timeslot switching is effected within the payload; and
assembling fixed length outgoing data packets from the outgoing **headers** stream and the outgoing data stream, and directing the outgoing data packets to those of the plurality of output data ports to which the packets...

8/3,K/53 (Item 31 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2004 WIPO/Univentio. All rts. reserv.

00300850 **Image available**
UPDATE MECHANISM FOR COMPUTER STORAGE CONTAINER MANAGER
MOYEN DE MISE A JOUR POUR MODULE DE GESTION D'ELEMENTS DE STOCKAGE D'ORDINATEURS
Patent Applicant/Assignee:
APPLE COMPUTER INC,
Inventor(s):
HARRIS Jared M,
RUBEN Ira L,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9519001 A1 19950713
Application: WO 95US196 19950104 (PCT/WO US9500196)
Priority Application: US 94177853 19940105

Designated States: AM AT [redacted] BB BG BR BY CA CH CN CZ DE DK [redacted] ES FI GB GE HU
JP KE KG KP KR KZ LK LR LT LU LV MD MG MN MW MX NL NO NZ PL PT RO RU SD
SE SI SK TJ TT UA UZ VN KE MW SD SZ AT BE CH DE DK ES FR GB GR IE IT LU
MC NL PT SE BF BJ CF CG CI CM GA GN ML MR NE SN TD TG
Publication Language: English
Fulltext Word Count: 119635

Fulltext Availability:
Claims

Claim
... types is tied into the
mechanism for accessing values, so that the type
associated with a value causes the appropriate code to
be executed to **access** the value, decompress it,
byte - swap it, and so on. The specific mechanism for
doing this is referred to herein as Dynamic Values.
Secondary Entities. In addition to the primary
entities...

8/3,K/54 (Item 32 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2004 WIPO/Univentio. All rts. reserv.

00270605 **Image available**
A METHOD AND APPARATUS FOR AUDIO TELECONFERENCING A PLURALITY OF PHONE CHANNELS
PROCEDE ET APPAREIL D'AUDIO TELECONFERENCE SUR UNE PLURALITE DE VOIES TELEPHONIQUES
Patent Applicant/Assignee:
MULTILINK INCORPORATED,
Inventor(s):
ALLEN Bruce S,
GARRISON Marshall B,
BRODSKY Philip S,
LEBLANC Richard E,
BAUN Philip J Jr,
MCCARTHY Gary R,
LEONDIRES Arthur P,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9418779 A1 19940818
Application: WO 94US1155 19940131 (PCT/WO US9401155)
Priority Application: US 9312028 19930201
Designated States: AT AU BB BG BR BY CA CH CN CZ DE DK ES FI GB HU JP KP KR
KZ LK LU LV MG MN MW NL NO NZ PL PT RO RU SD SE SK UA UZ VN AT BE CH DE
DK ES FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN ML MR NE SN
TD TG
Publication Language: English
Fulltext Word Count: 58194

Fulltext Availability:
Detailed Description

Detailed Description
... are doing a warm restart and if the DSP board is already in operation.

* Does the DSP/Host interface suffer from the big-endian/little- **endian** syndrome; i.e., does one side need to do **byte - swapping** ? If so, the host will do the **byte - swapping** .

6. Appendices
io The attached **header** files are snapshots of software documents. This document is not intended to represent the current or official version of those files. Refer to the source...

8/3,K/55 (Item 33 from file: 349)

DIALOG(R)File 349:PCT FULLTEXT
(c) 2004 WIPO/Univentio. All rts. reserv.

00259152
VIRTUAL NETWORK USING ASYNCHRONOUS TRANSFER MODE
RESEAU VIRTUEL UTILISANT UN MODE DE TRANSFERT ASYNCHRONE
Patent Applicant/Assignee:
  NETWORK EQUIPMENT TECHNOLOGIES INC,
Inventor(s):
  BURNETTE John Lindsay,
  NEWMAN Peter,
Patent and Priority Information (Country, Number, Date):
  Patent: WO 9407316 A1 19940331
  Application: WO 93US8674 19930914 (PCT/WO US9308674)
  Priority Application: US 92944682 19920914
Designated States: AU CA JP KR AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE
Publication Language: English
Fulltext Word Count: 61747

Fulltext Availability:
  Detailed Description

Detailed Description
... vp->vcte local;
  S->callee vp->vctEFpeer;
  S->Ipackets vp->v&e-ipackets;
  S->opackets vp->vcte opackets;
  atm
  settime(s->time);
  return;
  #ifdef little- **endian**
  svc **swappdu** (pdu, Ien)
  it-ruct xdu *Pdu;
  Int len;
  int reason = 0;
  strUct port addr elem *pae;
  Int
   All pdus have an Imi-hdr. The only thing In the **header**
   that must be swapped is the uJong lmi-cref.value. Do it
  now.

  ?0013
  Svc UtI. C
  445
  OS.REVERSE32(pdu->Imi.cref.vaii.ie...

8/3,K/56 (Item 34 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2004 WIPO/Univentio. All rts. reserv.

00234265 **Image available**
SYSTEM FOR DIVIDING PROCESSING TASKS INTO SIGNAL PROCESSOR AND DECISION-MAKING MICROPROCESSOR INTERFACING
SYSTEME DE SEPARATION DES TACHES DE TRAITEMENT EN TACHES POUR INTERFACAGE AVEC UN PROCESSEUR DE SIGNAUX ET UN MICROPROCESSEUR DE PRISE DE DECISION
Patent Applicant/Assignee:
  STAR SEMICONDUCTOR CORPORATION,
Inventor(s):
  ROBINSON Jeffrey I,
  ROUSE Keith,
  KRASSOWSKI Andrew J,
  MONTLICK Terry F,
Patent and Priority Information (Country, Number, Date):
  Patent: WO 9308524 A1 19930429
  Application: WO 92US8954 19921014 (PCT/WO US9208954)

Priority Application: [redacted]91776161 19911015
Designated States: AU CA JP KR AT BE CH DE DK ES FR GB GR IE IT LU MC NL SE
Publication Language: English
Fulltext Word Count: 219172
Fulltext Availability:
Claims

Claim
... data bus. For 16-and 24-bit modes, the most significant byte is leftjustified within the data word, with descending order of significance in lower **order** data bus **bytes** .
MODE[1] MODE[Q] DATA
0 0 8-bit
1 0 16-bit
X 1 24-bit
MODE[2] determines the byte or word ordering...W`124@ TYPE is a 24-bit integer data type. AR symbols are declared to be sdata, a union of all SPROC data types. The **header** file sprocdef.h defines the SPROC data types and function prototypes. It must be inchided in each C module that references SPROC data values. SMI supports applications using both Motorola-type (little **endian**) and Intel-type (big **endian**) **byte ordering** , The default **byte** , **ordering** is Motorola-type. To **change** the **byte** **ordering** , one must edit the file sprocdef h, or use the #define RiTEL statement or the define switch on the C compiler. To edit the file...

```
File 275:Gale Group Comp[redacted]r DB(TM) 1983-2004/Jun 15
         (c) 2004 The Gale Group
File 621:Gale Group New Prod.Annou.(R) 1985-2004/Jun 15
         (c) 2004 The Gale Group
File 636:Gale Group Newsletter DB(TM) 1987-2004/Jun 14
         (c) 2004 The Gale Group
File  16:Gale Group PROMT(R) 1990-2004/Jun 15
         (c) 2004 The Gale Group
File 160:Gale Group PROMT(R) 1972-1989
         (c) 1999 The Gale Group
File 148:Gale Group Trade & Industry DB 1976-2004/Jun 15
         (c)2004 The Gale Group
File 624:McGraw-Hill Publications 1985-2004/Jun 14
         (c) 2004 McGraw-Hill Co. Inc
File  15:ABI/Inform(R) 1971-2004/Jun 14
         (c) 2004 ProQuest Info&Learning
File 647:CMP  Computer Fulltext 1988-2004/Jun W1
         (c) 2004 CMP Media, LLC
File 674:Computer News Fulltext 1989-2004/Jun W2
         (c) 2004 IDG Communications
File 696:DIALOG Telecom. Newsletters 1995-2004/Jun 14
         (c) 2004 The Dialog Corp.
File 369:New Scientist 1994-2004/Jun W1
         (c) 2004 Reed Business Information Ltd.

Set     Items   Description
S1        508   (ENDIAN? OR (ORDER??? OR ARRANG?)(3N)BYTE? ?)(10N)(CONVERT?
                OR CONVERSION OR TRANSFORM? OR TRANSLAT? OR CHANG??? OR EXCH-
                ANG??? OR SWITCH??? OR SWAP???? OR MODIF???? OR MODIFICATION?
                ? OR ALTER??? OR ALTERATION? ? OR FLIP????)
S2        731   BYTE? ?(5N)(SWAP???? OR REORDER? OR RE()ORDER??? OR INTERC-
                HANG???)
S3      52756   HEADER? ?
S4       7296   LUT OR LUTS OR (LOOKUP OR LOOK()UP)()TABLE? ?
S5     606960   FILE? ?(5N)ACCESS??? OR FILESYSTEM? ? OR FILE()SYSTEM? ? OR
                FAT?? OR NTFS
S6         12   S1:S2(50N)S3
S7          0   S1:S2(50N)S4
S8         23   S1:S2(50N)S5
S9          0   S1:S2(100N)S4
S10        30   S1:S2(100N)(FILE? ?(5N)ACCESS???)
S11        46   S6:S10
S12        30   RD (unique items)
S13        30   S12 NOT PD>20020228
S14      1520   ENDIAN?
S15        21   S14(50N)S4:S5
S16        13   RD (unique items)
S17        11   S16 NOT S13
```

13/3,K/1 (Item 1 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2004 The Gale Group. All rts. reserv.

02521105 SUPPLIER NUMBER: 76611561 (USE FORMAT 7 OR 9 FOR FULL TEXT)
PATENT WATCH. (Industry Trend or Event)
Belgard, Rich
Microprocessor Report, 15, 5, 26
May, 2001
ISSN: 0899-9341 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 592 LINE COUNT: 00064

... store queue that it maintains for each byte accessed by a load independently of the other bytes, and determines the most recent store (in program **order**) to update that **byte** . Therefore, even if some bytes accessed by the load are **modified** by one store while other bytes are modified by another store, the forwarding mechanism will correctly assemble the bytes accessed by the load.
6,134,653
RISC processor architecture with high performance context switching in which one context can be loaded by a co-processor while another context is being **accessed** by an arithmetic logic unit
Filed : April 22, 1998 Issued: October 17, 2000
Inventors: Subhash Roy et al. Claims: 20
Assignee: TranSwitch
A RISC processor includes an ALU and a register...

13/3,K/2 (Item 2 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2004 The Gale Group. All rts. reserv.

02007812 SUPPLIER NUMBER: 18874604 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Open OS support boosts flexibility of RAID systems. (Data General's Clariion Series 3000, Zitel's CASD-II Enterprise and nStor's CR6e RAID systems) (Brief Article) (Product Announcement)
Lapolla, Stephanie
PC Week, v13, n46, p53(1)
Nov 18, 1996
DOCUMENT TYPE: Brief Article Product Announcement ISSN: 0740-1604
LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 444 LINE COUNT: 00037

... a dual-host fast SCSI interface and up to 512M bytes of cache memory. Cache can be configured into SSD (Solid State Disk) for fast **access** to frequently used **files** or as a dedicated SSD for clusters, officials said.
Including up to 17.2G **bytes** of hot- **swap** disk storage, the CASD-II is priced from $16,500 and is available now. nStor is shipping the CR6e, a six-bay unit holding 24G...

13/3,K/3 (Item 3 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2004 The Gale Group. All rts. reserv.

01964155 SUPPLIER NUMBER: 18246132 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Verite: a programmable 3D chip. (Rendition's hybrid chip) (includes related article on price, availability) (Product Information)
Gwennap, Linley
Microprocessor Report, v10, n6, p1(6)
May 6, 1996
ISSN: 0899-9341 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 5043 LINE COUNT: 00394

... straightforward encoding. Loads and branches each have a single delay slot, although the hardware provides load interlocks, unlike the R3000. Data is stored in big- **endian** format, but the DMA engine supports

endian **swapping** for c[redacted]atibility with little- **endian** [redacted]6 processors. As in the MIPS architecture, only a single addressing mode, register+offset, is provided. These features give the Verite CPU a general-purpose...

...other RISC) core, but the company found it necessary to add a few optimizations to enhance graphics performance. A key feature is the large register **file** : each instruction can **access** any of 256 registers for its source or destination fields. Of these, 128 are general-purpose registers, giving Verite more than four times the register...

13/3,K/4 (Item 4 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2004 The Gale Group. All rts. reserv.

01891300 SUPPLIER NUMBER: 17990724 (USE FORMAT 7 OR 9 FOR FULL TEXT)
DCE: an environment for secure client/server computing. (Open Software Foundation's Distributed Computing Environment) (Technology Information)
Kong, Michael M.
Hewlett-Packard Journal, v46, n6, p6(10)
Dec, 1995
ISSN: 0018-1153 LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 8390 LINE COUNT: 00704

... format. For these primitive types, the format that governs a particular PDU is indicated as part of the data representation format label in the PDU **header** . On any given hardware architecture, the DCE library will send outgoing data in the representations native to that architecture. If the receiving host has different native representations, its DCE library will convert incoming data (for example, by **swapping** **bytes** in integers) as necessary. DCE RPC thus has what may be called a multicanonical approach to data representation. This approach tends to minimize data conversion...

13/3,K/5 (Item 5 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2004 The Gale Group. All rts. reserv.

01834837 SUPPLIER NUMBER: 17412667
Hot on the trail with a bloodhound called REXX. (OS/2 programming) (Tutorial)
Mahoney, Robert
OS2 Professional, v3, n7, p55(8)
July 17, 1995
DOCUMENT TYPE: Tutorial ISSN: 1069-6814 LANGUAGE: English
RECORD TYPE: Abstract

...ABSTRACT: a different parameter. Also, while the simple parameters are little-endian, datastream data is passed in big-endian format. Although the Intel architecture is little- **endian** , Bloodhound **headers** include a macro to do the **conversion** .

13/3,K/6 (Item 6 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2004 The Gale Group. All rts. reserv.

01829549 SUPPLIER NUMBER: 17277985 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Xbase gains lease on life. (Visual dBASE, Visual FoxPro) (includes related article on continuing use of Xbase as data language) (Software Review) (Evaluation)
Taschek, John
PC Week, v12, n34, p69(3)
August 28, 1995
DOCUMENT TYPE: Evaluation ISSN: 0740-1604 LANGUAGE: English
RECORD TYPE: Fulltext; Abstract
WORD COUNT: 2546 LINE COUNT: 00235

... hard drive. We t[redacted]ed Visual dBASE and Visual Fox[redacted] running under MS-DOS 6.22 and Microsoft Windows for Workgroups 3.11 with a 20M- **byte** permanent **swap** file and 32-bit disk and **file** **access** turned on with the default cache size setting.

PC Week Labs Corporate Buyers' Advisory: Programmable Databases Visual dBASE 5.5 for Windows Client/Server Edition...

13/3,K/7 **(Item 7 from file: 275)**
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2004 The Gale Group. All rts. reserv.

01782322 SUPPLIER NUMBER: 16867123 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Reporting tool combines C/S strength, user interface; SQLAssist ProReports provides powerful querying capabilities. (Software Interfaces' version 1.3) (includes related article on test methods) (Software Review) (Evaluation)
Taschek, John
PC Week, v12, n19, p69(2)
May 15, 1995
DOCUMENT TYPE: Evaluation ISSN: 0740-1604 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT
WORD COUNT: 1276 LINE COUNT: 00107

... 500M-byte hard drive. We ran our tests under MS-DOS 6.22 and Microsoft Corp.'s Windows for Workgroups 3.11, with a 20M- **byte** permanent **swap** file and 32-bit **file** and disk **access** enabled.

13/3,K/8 **(Item 8 from file: 275)**
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2004 The Gale Group. All rts. reserv.

01728619 SUPPLIER NUMBER: 16433149 (USE FORMAT 7 OR 9 FOR FULL TEXT)
New report writers provide improved access to data: trio offers specialized tools. (Borland's ReportSmith for Windows 2.5, Concentric Data Systems Inc's R&R Report Writer 6.0, Crystal's Crystal Reports Professional 4.0) (includes related articles on test methodology and the advantages of stand-alone report writers) (Software Review) (Evaluation)
Taschek, John
PC Week, v12, n5, p81(4)
Feb 6, 1995
DOCUMENT TYPE: Evaluation ISSN: 0740-1604 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 3380 LINE COUNT: 00264
>>>DLCT105: TYPE/DISPLAY error

13/3,K/20 **(Item 1 from file: 636)**
DIALOG(R)File 636:Gale Group Newsletter DB(TM)
(c) 2004 The Gale Group. All rts. reserv.

03357513 Supplier Number: 46905692 (USE FORMAT 7 FOR FULLTEXT)
ENTEGRA LTD: Industry's first Dual 'C80 PCI board available from Pentek
M2 Presswire, pN/A
Nov 20, 1996
Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 631

... allows the board to support multiple video standards, including but not limited to RS-170, NTSC, PAL, RGB and digital (camera).

Selectable Big or Little **Endian** Mode The Model 7280 proprietary **endian** **swapping** logic allows the processor to operate in either big or little endian mode while interfacing to the little endian PCI bus. Two 2-pin **headers** control the **endian** mode of each processor and set up the **endian** **swapping** logic between the processor core and the PCI interface logic to control the byte lane multiplexing during data transfers of

various sizes.
Initially, the Model...

13/3,K/21 (Item 2 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)
(c) 2004 The Gale Group. All rts. reserv.

03112321 Supplier Number: 46362920 (USE FORMAT 7 FOR FULLTEXT)
Verite: A Programmable 3D Chip
Microprocessor Report, v10, n6, pN/A
May 6, 1996
Language: English Record Type: Fulltext
Document Type: Newsletter; Refereed; Trade
Word Count: 4702

... straightforward encoding. Loads and branches each have a single delay slot, although the hardware provides load interlocks, unlike the R3000. Data is stored in big- **endian** format, but the DMA engine supports **endian swapping** for compatibility with little- **endian** x86 processors. As in the MIPS architecture, only a single addressing mode, register+offset, is provided. These features give the Verite CPU a general-purpose...

...other RISC) core, but the company found it necessary to add a few optimizations to enhance graphics performance. A key feature is the large register **file** : each instruction can **access** any of 256 registers for its source or destination fields. Of these, 128 are general-purpose registers, giving Verite more than four times the register...

13/3,K/22 (Item 1 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)
(c) 2004 The Gale Group. All rts. reserv.

05641749 Supplier Number: 50087597 (USE FORMAT 7 FOR FULLTEXT)
QNX solves alignments
Electronics Times, pN/A
June 8, 1998
Language: English Record Type: Fulltext
Article Type: Article
Document Type: Magazine/Journal; Trade
Word Count: 269

... both."
For routines supported by the RTOS, drivers can be written independently of byte ordering supported by an individual processor. Macros defined in the driver **header** files determine how I/O requests to hardware are handled on each platform. For example, a peripheral may organise its I/O registers as 32bit big-endian values which are not aligned to 32bit boundaries. This can be forced by using the defined primitives.
On a big- **endian** PowerPC processor, the request would not be **byte** - **swapped** by the RTOS but the implementation may add code to handle the unaligned access. On an x86, an I/O request is handled from an...

13/3,K/23 (Item 2 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)
(c) 2004 The Gale Group. All rts. reserv.

05601598 Supplier Number: 48476737 (USE FORMAT 7 FOR FULLTEXT)
Moto targets multimedia; IBM speed -- Moto, IBM split on PowerPC direction
Wirbel, Loring; Cataldo, Anthony
Electronic Engineering Times, p1
May 11, 1998
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 1527

... the permute operation, reminiscent of the complex data-swizzling instructions in the architecture developed by MicroUnity (Sunnyvale, Calif.). The instruction can essentially perform an arbitrary **reordering** of the **bytes** , words or double words in a 128-bit register in one cycle, placing the result in another register. Such an operation could extract or replace the **header** of a communications packet in a single cycle, or slash the time required for the messy pixel reordering required by MPEG-2 decoding.

The combination...

13/3,K/24 (Item 3 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)
(c) 2004 The Gale Group. All rts. reserv.

04688375 Supplier Number: 46900661 (USE FORMAT 7 FOR FULLTEXT)
Open OS support boosts flexibility of RAID systems
PC Week, p053
Nov 18, 1996
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Tabloid; General Trade
Word Count: 417

... a dual-host fast SCSI interface and up to 512M bytes of cache memory. Cache can be configured into SSD (Solid State Disk) for fast **access** to frequently used **files** or as a dedicated SSD for clusters, officials said.

Including up to 17.2G **bytes** of hot- **swap** disk storage, the CASD-II is priced from $16,500 and is available now. nStor is shipping the CR6e, a six-bay unit holding 24G...

13/3,K/25 (Item 4 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)
(c) 2004 The Gale Group. All rts. reserv.

03965238 Supplier Number: 45749119 (USE FORMAT 7 FOR FULLTEXT)
Xbase gains lease on life
PC Week, p69
August 28, 1995
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Tabloid; General Trade
Word Count: 2551

... hard drive. We tested Visual dBASE and Visual FoxPro running under MS-DOS 6.22 and Microsoft Windows for Workgroups 3.11 with a 20M- **byte** permanent **swap** file and 32-bit disk and **file access** turned on with the default cache size setting.

PC Week Labs Corporate Buyers' Advisory: Programmable Databases

Visual dBASE 5.5 for Windows Client/Server Edition...

13/3,K/26 (Item 1 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2004 The Gale Group. All rts. reserv.

07299061 SUPPLIER NUMBER: 15548569 (USE FORMAT 7 OR 9 FOR FULL TEXT)
All for one and one for all. (review of Microsoft Office Professional 4.3, Lotus SmartSuite for Windows 2.1 and Borland Office for Windows 2.0 integrated software) (includes related articles on an executive summary, testing methods used, summary of test results, how office suites manage system resources and data sharing capabilities of office suites) (Software Review) (overview of three evaluations of integrated office suites) (Evaluation)
Marshall, Patrick; Eva, Elizabeth
InfoWorld, v16, n26, p104(13)
June 27, 1994

DOCUMENT TYPE: Evaluatio[redacted] ISSN: 0199-6649 LANGU[redacted]: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 6912 LINE COUNT: 00559

... utilization tests on a 33-MHz Gateway i486/DX with 8MB of RAM and a 162MB IDE hard drive. We set a permanent 11,748- **byte** Windows **swap file** using 32-bit **access** . We used Norton SystemWatch, from Symantec Corp.'s Norton Utilities 8.0, to monitor system resources.
We performed our usability tests on the same platform...

13/3,K/27 (Item 2 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2004 The Gale Group. All rts. reserv.

05181999 SUPPLIER NUMBER: 10764914 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Group seeks shrink-wrapped software for Mips RX000. (consortium to define Application Program Interface)
[illegible], Sherman
EDN, v36, n10A, p3(2)
May 16, 1991
ISSN: 0012-7515 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 1087 LINE COUNT: 00086

... say others. DOS programs and files, for example, use little endian byte ordering, says SCO vice president Scott McGregor. As a result, he says, DOS **files** can only be **accessed** on a Unix network by those machines that also use little **endian byte ordering** . A file **converter** or **translator** is required for machines such as the Sun SPARC, which use a big endian byte-order scheme, he claims.
Without an identical byte-ordering scheme...

13/3,K/28 (Item 1 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)
(c) 2004 ProQuest Info&Learning. All rts. reserv.

01820128 04-71119
NFS running just to stay in place
Trowbridge, Dave
Computer Technology Review v19n4 PP: 1, 14 Apr 1999
ISSN: 0278-9647 JRNL CODE: CTN
WORD COUNT: 1054

...TEXT: either UDP or TCP).

NFS is also machine and language independent because it uses Sun's External Data Representation (XDR) standard, which defines the size, **byte order** , and alignment of basic data types, enabling data to be **exchanged** between systems with different **byte ordering** conventions. An NFS server process uses a Virtual **File System** (VFS) to present remote data and **file systems** in a consistent manner and a NFS client then translates this VFS interface to the semantics of the local **file system** , such as Microsoft's **NTFS** in Windows NT.

An NFS server is generally merely a process in a Unix machine, although companies such as Network Appliance Inc. manufacture dedicated network...

13/3,K/29 (Item 1 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext
(c) 2004 CMP Media, LLC. All rts. reserv.

01161012 CMP ACCESSION NUMBER: EET19980511S0001
Moto targets multimedia; IBM speed - Moto, IBM split on PowerPC direction
Anthony Cataldo And Loring Wirbel
ELECTRONIC ENGINEERING TIMES, 1998, n 1006, PG1
PUBLICATION DATE: 980511

JOURNAL CODE: EET LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: News
WORD COUNT: 1534

... the permute operation, reminiscent of the complex data-swizzling instructions in the architecture developed by MicroUnity (Sunnyvale, Calif.). The instruction can essentially perform an arbitrary **reordering** of the **bytes** , words or double words in a 128-bit register in one cycle, placing the result in another register. Such an operation could extract or replace the **header** of a communications packet in a single cycle, or slash the time required for the messy pixel reordering required by MPEG-2 decoding.

The combination...

13/3,K/30 (Item 2 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext
(c) 2004 CMP Media, LLC. All rts. reserv.

00651049 CMP ACCESSION NUMBER: CRN19891002S3016
LAST IN SERIES ON RISC PROCESSOR WARS - RISC awaits UNIX resolution
JOHN M. DODGE
COMPUTER RESELLER NEWS, 1989, n 335, 84
PUBLICATION DATE: 891002
JOURNAL CODE: CRN LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: SOF
WORD COUNT: 1613

... regard, UNIX is unique.
"UNIX has distinguished itself as a system whose design point is heterogeneity. It's associated with hundreds of utilities, gateways, common **file access** methods. The design point for OS/2 is not heterogeneity. It runs on the Intel architecture and nothing else," he said. He added that Lotus...

...some of the technical problems are political) remain. For example, just within the Mips platform, DEC's implementation differs from the other OEMs because it **changed** the **byte ordering** of the chip set. That means Ultrix applications must be substantially modified to run on other Mips platforms if they can run at all.

```
File   8:Ei Compendex(R) 1970-2004/Jun W1
         (c) 2004 Elsevier Eng.  Info. Inc.
File  35:Dissertation Abs Online 1861-2004/May
         (c) 2004 ProQuest Info&Learning
File 239:Info. Sci. & Tech. Abs. 1966-2004/May 14
         (c) 2004 EBSCO Publishing
File  65:Inside Conferences 1993-2004/Jun W2
         (c) 2004 BLDSC all rts. reserv.
File   2:INSPEC 1969-2004/Jun W1
         (c) 2004 Institution of Electrical Engineers
File  94:JICST-EPlus 1985-2004/May W4
         (c)2004 Japan Science and Tech Corp(JST)
File 483:Newspaper Abs Daily 1986-2004/Jun 11
         (c) 2004 ProQuest Info&Learning
File   6:NTIS 1964-2004/Jun W2
         (c) 2004 NTIS, Intl Cpyrght All Rights Res
File 144:Pascal 1973-2004/Jun W1
         (c) 2004 INIST/CNRS
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
File  34:SciSearch(R) Cited Ref Sci 1990-2004/Jun W1
         (c) 2004 Inst for Sci Info
File  99:Wilson Appl. Sci & Tech Abs 1983-2004/May
         (c) 2004 The HW Wilson Co.
File 583:Gale Group Globalbase(TM) 1986-2002/Dec 13
         (c) 2002 The Gale Group
File 266:FEDRIP 2004/Apr
         Comp & dist by NTIS, Intl Copyright All Rights Res
File  95:TEME-Technology & Management 1989-2004/May W4
         (c) 2004 FIZ TECHNIK
File 438:Library Lit. & Info. Science 1984-2004/May
         (c) 2004 The HW Wilson Co

Set      Items   Description
S1          28   (ENDIAN? OR (ORDER??? OR ARRANG?)(3N)BYTE? ?)(10N)(CONVERT?
                 OR CONVERSION OR TRANSFORM? OR TRANSLAT? OR CHANG??? OR EXCH-
                 ANG??? OR SWITCH??? OR SWAP???? OR MODIF???? OR MODIFICATION?
                 ? OR ALTER??? OR ALTERATION? ? OR FLIP????)
S2          39   BYTE? ?(5N)(SWAP???? OR REORDER? OR RE()ORDER??? OR INTERC-
                 HANG???)
S3       12331   HEADER? ?
S4       11999   LUT OR LUTS OR (LOOKUP OR LOOK()UP)()TABLE? ?
S5      730692   FILE? ?(5N)ACCESS??? OR FILESYSTEM? ? OR FILE()SYSTEM? ? OR
                 FAT?? OR NTFS
S6           4   S1:S2 AND S3:S5
S7           2   RD (unique items)
S8         133   ENDIAN?
S9           6   S8 AND S3:S5
S10          3   (S2 OR S8) AND TABLE? ?
S11         11   S7 OR S9:S10
S12          9   RD (unique items)
```

12/5/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)
(c) 2004 Elsevier Eng. Info. Inc. All rts. reserv.

06777967 E.I. No: EIP04138083473
Title: Embedded linux implementation on a commercial digital TV system
Author: Moon, Sang-Pil; Kim, Joo-Won; Bae, Kuk-Ho; Lee, Jae-Cheon; Seo, Dae-Wha
Corporate Source: Sch. of Elec. Eng. and Comp. Sci. Kyungpook National University, Daegu, South Korea
Source: IEEE Transactions on Consumer Electronics v 49 n 4 November 2003. p 1402-1407
Publication Year: 2003
CODEN: ITCEDA ISSN: 0098-3063
Language: English
Document Type: JA; (Journal Article) Treatment: T; (Theoretical)
Journal Announcement: 0403W5
Abstract: A Digital TV system is necessary for not only video and audio, but also data processing. Especially in the case of bidirectional broadcasting, it should manage the return channel created by the Internet, PSTN, and so on. Because of many functionalities and multitasking jobs, it needs an Operating System. Embedded Linux, as open source program can increase cost effectiveness in the market and has many advantages-reusable device drivers and application programs, more convenient development environment using shell and **file system** , and easy resolution of problem within the Open Source Community. In this paper, we modified the embedded Linux kernel and the cross development environment for a big-**endian** system, redesigned device drivers for kernel execution, and configured system memory map in order to load the Linux kernel. Also we developed a device driver for the entire system control. 12 Refs.
Descriptors: *Digital television; Computer operating systems; Embedded systems; Data storage equipment; Television broadcasting; Internet; Multiprogramming; Cost effectiveness; Marketing; Liquid crystal displays
Identifiers: Embedded linux kernel; Bidirectional broadcasting; Reusable device drivers
Classification Codes:
716.4 (Television Systems & Equipment); 723.5 (Computer Applications); 722.1 (Data Storage, Equipment & Techniques); 723.1 (Computer Programming); 911.2 (Industrial Economics); 911.4 (Marketing)
716 (Electronic Equipment, Radar, Radio & Television); 723 (Computer Software, Data Handling & Applications); 722 (Computer Hardware); 911 (Cost & Value Engineering; Industrial Economics)
71 (ELECTRONICS & COMMUNICATION ENGINEERING); 72 (COMPUTERS & DATA PROCESSING); 91 (ENGINEERING MANAGEMENT)

12/5/4 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC
(c) 2004 Institution of Electrical Engineers. All rts. reserv.

7878042 INSPEC Abstract Number: C2004-04-5260-007
Title: Real-time signal analysis and real-time Linux. II
Author(s): Sherer, M.
Journal: Dr. Dobb's Journal vol.28, no.8 p.54, 56, 58, 60-1
Publisher: CMP Media LLC,
Publication Date: Aug. 2003 Country of Publication: USA
CODEN: DDJSDM ISSN: 1044-789X
SICI: 1044-789X(200308)28:8L.54:RTSA;1-V
Material Identity Number: B719-2003-007
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: Hard real-time systems need to immediately capture, analyze, and act on incoming signals. In the first we focused on capturing real-time signals and visualizing data using a simple Java GUI. We simplify both the real-time and Java code and add a digital filter. To make the code changes necessary to enable filtering, we need to include the Controls Kit **headers** , and then add a couple more declarations up front. Controls Kit variables can be directly controlled with userspace utilities, so we don't need extra

FIFOs, sigaction() callb[redacted]s, shared structural protocol [redacted]ining the data, and (above all) the **endian** reordering.
Subfile: C
Descriptors: digital filters; graphical user interfaces; harmonic analysis; Java; real-time systems; signal processing; Unix
Identifiers: real-time systems; Java; GUI; digital filter; Controls Kit **headers** ; real-time signal analysis; real-time Linux
Class Codes: C5260 (Digital signal processing); C6110J (Object-oriented programming); C6150J (Operating systems); C5240 (Digital filters); C6180G (Graphical user interfaces)
Copyright 2004, IEE

12/5/5 **(Item 3 from file: 2)**
DIALOG(R)File 2:INSPEC
(c) 2004 Institution of Electrical Engineers. All rts. reserv.

6489845 INSPEC Abstract Number: B2000-03-6120D-033, C2000-03-1260C-020
Title: Cryptanalysis of a reduced version of the block cipher E2
Author(s): Matsui, M.; Tokita, T.
Author Affiliation: Center for Inf. Technol. R&D, Mitsubishi Electr. Corp., Kanagawa, Japan
Conference Title: Fast Software Encryption. 6th International Workshop, FSE'99. Proceedings p.71-80
Editor(s): Knudsen, L.
Publisher: Springer-Verlag, Berlin, Germany
Publication Date: 1999 Country of Publication: Germany viii+316 pp.
ISBN: 3 540 66226 X Material Identity Number: XX-1999-02370
Conference Title: Fast Software Encryption. 6th International Workshop, FSE'99
Conference Date: 24-26 March 1999 Conference Location: Rome, Italy
Language: English Document Type: Conference Paper (PA)
Treatment: Theoretical (T)
Abstract: This paper deals with truncated differential cryptanalysis of the 128-bit block cipher E2, which is an AES candidate designed and submitted by NTT. Our analysis is based on byte characteristics, where a difference of two bytes is simply encoded into one bit information "0" (the same) or "1" (not the same). Since E2 is a strongly byte-oriented algorithm, this bytewise treatment of characteristics greatly simplifies a description of its probabilistic behavior and noticeably enables us an analysis independent of the structure of its (unique) **lookup table** . As a result, we show a non-trivial seven-round byte characteristic, which leads to a possible attack of E2 reduced to eight rounds without IT and FT by a chosen plaintext scenario. We also show that by a minor **modification** of the **byte order** of output of the round function - which does not reduce the complexity of the algorithm nor violate its design criteria at all - a non-trivial nine-round byte characteristic can be established, which results in a possible attack of the modified E2 reduced to ten rounds without IT and FT, and reduced to nine rounds with IT and FT. Our analysis does not have a serious impact on the full E2, since it has twelve rounds with IT and FT; however, our results show that the security level of the modified version against differential cryptanalysis is lower than the designers' estimation. (5 Refs)
Subfile: B C
Descriptors: computational complexity; cryptography; probability; table lookup
Identifiers: E2 block cipher; truncated differential cryptanalysis; 128-bit block cipher; AES candidate; NTT; byte-oriented algorithm; probabilistic behavior; **lookup table** ; non-trivial byte characteristic; seven-round byte characteristic; attack; chosen plaintext; output order; round function; nine-round byte characteristic; IT; FT; security level; initial transformation; final transformation; complexity
Class Codes: B6120D (Cryptography); C1260C (Cryptography theory)
Copyright 2000, IEE

12/5/6 **(Item 4 from file: 2)**
DIALOG(R)File 2:INSPEC

(c) 2004 Institution of [redacted]ctrical Engineers. All rts. re[redacted]v.

04168471 INSPEC Abstract Number: C9207-6110B-037
Title: Portability of programs written in C language
Author(s): Calia, E.; Gai, S.; Montessoro, P.L.
Author Affiliation: Dipartimento di Automatica e Inf., Politecnico di Torino, Italy
Journal: Rivista di Informatica vol.22, no.1 p.43-60
Publication Date: Jan.-March 1992 Country of Publication: Italy
CODEN: RIINDL ISSN: 0390-668X
Language: Italian Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: A discussion is given on portability problems of programs written in C language with respect to different operating systems and machine architectures. Coding methodologies for portability are presented. C compilers impose limitations related to the preprocessor, the symbol **table** , or to the intermediate code generation. Not all C implementations support the same standard library functions; a generalized technique is presented to write simple interface files that make programs compatible with libraries belonging to different compilers. Since in many multiprocessing applications the fork function is very important, a brief discussion is presented to explain why it is widely used by the Unix operating system, whereas it is not supported by VAX/VMS. Many compilers optimize static and dynamic data structure allocation for the hardware of the host machine. The criteria to define unions and structs that ensure that they will work under all C implementations are presented with many examples. The problem of little- **endian** vs. big- **endian** architectures is also addressed. Almost all compilers allow implicit type casting in assignments and in parameter passing. When programs are compiled on machines with different word size this may create multifunctionings detectable only at run time. The portability implications of the new ANSI standard for C language are also discussed. (14 Refs)
Subfile: C
Descriptors: C language; data structures; operating systems (computers); program compilers; software portability; standards; subroutines
Identifiers: portability problems; C language; operating systems; machine architectures; C compilers; preprocessor; symbol **table** ; intermediate code generation; C implementations; standard library functions; simple interface files; multiprocessing applications; fork function; Unix operating system; VAX/VMS; dynamic data structure allocation; unions; structs; little- **endian** ; big- **endian** architectures; implicit type casting; parameter passing; portability implications; ANSI standard
Class Codes: C6110B (Software engineering techniques); C6140D (High level languages); C6150C (Compilers, interpreters and other processors); C6150J (Operating systems); C6120 (File organisation)

12/5/7 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC
(c) 2004 Institution of Electrical Engineers. All rts. reserv.

01427289 INSPEC Abstract Number: C79033427
Title: The microcomputer TM 990/189
Journal: Funkschau vol.51, no.15 p.885-6
Publication Date: 20 July 1979 Country of Publication: West Germany
CODEN: FUSHA2 ISSN: 0016-2841
Language: German Document Type: Journal Paper (JP)
Treatment: General, Review (G)
Abstract: Discusses the single-board Texas Instruments microcomputer about 30 ICs, a 4 kbyte ROM and a 1 kbyte RAM, a symbolic assembler and some sophisticated circuit facilities for parity 'jumps', **swap bytes** , etc. Its heart, the TMS 9980 CPU is a 16 bit microprocessor with 14 address leads and 6 interrupts, the RAM doubling up as the external register. A **table** quotes the functions and store stacking of the monitoring sub-programs. (0 Refs)
Subfile: C
Descriptors: computer architecture; microcomputers; microprocessor chips
Identifiers: microcomputer TM 990/189; Texas Instruments; single board

microcomputer; TMS 9980 [redacted]bit microprocessor; computer a[redacted]itecture
Class Codes: C5220 (Computer architecture); C5250 (Microcomputer
Techniques); C5430 (Microcomputers)

12/5/8 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus
(c)2004 Japan Science and Tech Corp(JST). All rts. reserv.

00723775 JICST ACCESSION NUMBER: 89A0390556 FILE SEGMENT: JICST-E
A proposal of intermediate language between Japanese word-processors and page description languages.
WAKATORI RIKUO (1)
(1) Nihon'yunishisu
Joho Shori Gakkai Kenkyu Hokoku, 1989, VOL.89,NO.36(MIC-55), PAGE.55-5,1-8
JOURNAL NUMBER: Z0031BAO ISSN NO: 0919-6072
UNIVERSAL DECIMAL CLASSIFICATION: 681.3.02:651.2
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: The author proposes an intermediate language (cps) bridges between word-processors and page description language (PDL). This keeps compatibility in the output data stream, especially in multi byte Kanji character codes at **file system** . A key feature of this proposal is that a document prolog consists of short form of PostScript language and code conversion rules from two **byte interchange** code to internal code in a representation device. The document prolog is sent to a presentation device with document body. NOTE: All descriptions were written is Japanese, but English version will be supported by the author if requested.(author abst.)